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REMARKS

The Examiner is thanked for his/her careful and very thorough Office Action. No claims are amended at this time. All rejections are hereby respectfully traversed. Favorable reconsideration of the claims is respectfully requested.

Art Rejections

It is respectfully submitted that Kaiser's teaching does not teach the limitations in the claims of the present application. Specifically, Applicant respectfully submits that what Examiner refers to as a "less extreme page fault" (for example, at page 2 of the present Office action) is not a page fault, but is instead a situation where the address translation of command data is not found in the TLB. This only means that the address translation is missing. It does not mean that the data is not present, and it is not a page fault. Kaiser does not describe this situation as a page fault.

Kaiser does describe a page fault in other circumstances--"When a page is accessed by a processor and it is not in real memory, a page fault interrupt occurs and software brings in the page from disk and maps it to a real page in memory." It is specifically noted that the address translation Examiner refers to as a "less extreme page fault" is not, in fact, a page fault. Address translation is performed before the system page table is checked for the needed data. Without performing address translation first, the memory controller (or graphics processor or host processor) would not know what physical address to look in to find the data.

Kaiser does describe a way to alleviate the need to have the host processor perform these address translations. However, Kaiser explicitly uses the host processor when a page fault occurs. It is respectfully submitted that Examiner's characterization of the address translation as a page fault is incorrect. Because of this incorrect characterization, it is respectfully submitted that Kaiser does not teach or suggest, for example, the limitations of claim 1. This is discussed more fully below, with reference to FIGs 1 and 2 of Kaiser.

Kaiser executes graphics processing functions in a graphics processor (206) located in a memory controller 204 attached to a host processor's 12 bus 14, 16. Kaiser says it works by translating virtual (or effective) addresses contained in command blocks (sent to the graphics processor) into real addresses, so that access is made to real addresses in memory (i.e., system memory 24 of FIG. 2). (See generally the summary, col. 3, lines 50-55.)

To do this, the memory controller of Kaiser uses a Translation Lookaside Buffer (TLB 220) to store recently used address translations. The TLB entries are compared to addresses in the commands sent to the graphics processor. If there is no match, this means the translation from the virtual address to a real address is not in the TLB. In short, it is unknown yet where the data resides, and a correct address translation must be found.

The memory controller must take another action to find the proper real address of the data it needs. It performs a page walk (as described at col. 5, lines 50-55): "Memory controller 204 fetches cache lines from the system page table on an as-needed basis to find an effective real address translation..."

At this point, the memory controller now has the address translation it needs to translate the virtual address sent to the graphics processor into a real address for data stored in system memory 24. Because this was a virtual address, some of the virtual memory will not actually be in system memory, but may instead be on the disk.

If the address is not in system memory, and is instead on the disk, then a page fault occurs.

Hence, what Examiner refers to as a "less extreme page fault" is not a page fault at all. It appears that Examiner is referring to the fact that there is no TLB entry that gives a translation for the virtual address sent to the graphics processor. When no such translation exists, a translation is needed. Hence, the memory controller performs a page walk and "fetches cache lines form the system page table on an as-needed basis to find an effective real address translation." This activity is, respectfully, not a page fault.

Only once that address translation is known can the memory controller actually attempt to access the data. Because it is translating a virtual memory address, some virtual addresses will map to system memory (which Kaiser

does not describe as a page fault) and some will map to the disk (which Kaiser does describe as a page fault). If the data sought, after translation, is found to exist in system memory, then Kaiser does not call this a page fault--it simply fetches the data. If, however, the data is not in system memory and is on the disk, then Kaiser describes handling the page fault. It is noted that Kaiser explicitly requires host processor assistance to handle the page fault.

The advantage of Kaiser is that it can translate these addresses without invoking the host processor. See, for example, col. 4, lines 15-19: "It is an advantage of the present invention that 3D graphics processing may be efficiently accomplished by an auxiliary function processor in a controller connected to the processor bus, without the overhead of the processor translating the addresses in the command blocks to real addresses...."

Kaiser does not, however, remove the host processor from the equation when an actual page fault occurs. Kaiser states the required involvement of the host processor at col. 6, lines 3-29.

Hence, Kaiser does not remove the host processor from page faults. It instead removes the host processor from translating the virtual addresses to real addresses. But after such a translation occurs, the system page table must be checked to find out if the data is actually stored in the system memory (which does not require a page fault) or if the data is on the disc (which does cause a page fault). When a page fault occurs in Kaiser, Kaiser must involve the host processor.

Hence, Applicant respectfully submits that Kaiser does not teach or suggest the claimed limitations of,

1. (original): A computer system, comprising:

a graphics accelerator unit which manages page faulting of texture data invisibly to the host processor.

Since there appear to be no circumstances under which Kaiser manages page faulting of texture data invisibly to the host processor, Applicant respectfully submits that all independent claims 1, 2, 3, 4, 7, 14, 15, 17, 20,

and 22 are distinguished from the cited references. Favorable reconsideration of the claims is respectfully requested.

Because of their dependence on allowable claims, all dependent claims are therefore believed allowable.

Favorable reconsideration is respectfully requested.

Conclusion

Thus, all grounds of rejection and/or objection are traversed or accommodated, and favorable reconsideration and allowance are respectfully requested. The Examiner is requested to telephone the undersigned attorney or Robert Groover for an interview to resolve any remaining issues.

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Respectfully submitted,

Patrick C. R. Holmes, Reg. #46,380
Attorney for Applicant

Customer Number 29106
Groover & Holmes
PO Box 802889
Dallas, TX 75380
Tel: 972-980-5840
fax: 972-980-5841